CLAIMS

The invention is claimed as follows:

1. A clock and data regenerator:

a first sampling flip-flop having a data input for receiving a data signal, having a clock input for receiving a first clock signal having a clock period corresponding to a duration of two bits of the data signal, and having an output;

a second sampling flip-flop having a data input for receiving the data signal, having a clock input for receiving a second clock signal which is phase-shifted by 180° with respect to the first clock signal, and having an output;

a third sampling flip-flop serving as a reference sampling flip-flop, the third sampling flip-flop having a data input for receiving the data signal, having a clock input for receiving a third clock signal which is phase-shifted by 90° with respect to at least one of the first and second clock signals, and having an output;

a fourth sampling flip-flop serving as a reference sampling flip-flop, the fourth sampling flip-flop having a data input for receiving the data signal, having a clock input for receiving a fourth clock signal which is phase-shifted by 180° relative to the third clock signal, and having an output;

a first EXOR element having a first input connected to the output of the first sampling flip-flop, having a second input connected to the output of the third sampling flip-flop, and having an output;

a second EXOR element having a first input connected to the output of the second sampling flip-flop, having a second input connected to the output of the third sampling flip-flop, and having an output;

a third EXOR element having a first input connected to the output of the second sampling flip-flop, having a second input connected to the output of the fourth sampling flip-flop, and having an output;

a fourth EXOR element having a first input connected to the first sampling flip-flop, having a second input connected to the output of the fourth sampling flip-flop, and having an output;

an addition and comparison circuit for combining the output of the first EXOR element with the output of the third EXOR element to produce a first result, for combining the output of the second EXOR element with the output of the fourth EXOR element to produce a second result, and for comparing the first and second results to produce a phase regulating signal which is then filtered; and

an oscillator, wherein the filtered phase regulating signal controls a frequency of the oscillator.

2. A clock and data regenerator as claimed in claim 1, wherein the addition and comparison circuit includes first and second adders and a comparison circuit, the outputs of the first and third EXOR elements being combined in the first adder to produce the first result, the outputs of the second and fourth EXOR elements being combined in the second adder to produce the second result, and the first and second results being compared in the comparison circuit.

3. A clock and data regenerator as claimed in claim 2, wherein a subtractor designed as a low-pass filter is provided as the comparison circuit.

4. A clock and data regenerator as claimed in claim 1, further comprising two further sampling stages and two further reference sampling stages having clock inputs for receiving clock signals each shifted by 45°, a duration of the clock signals corresponding to a duration of four bits of the data signal, and further comprising four pairs of EXOR elements and a further addition and comparison circuit which adds corresponding phase signals of the four pairs of EXOR elements and compares the added signals with one another.